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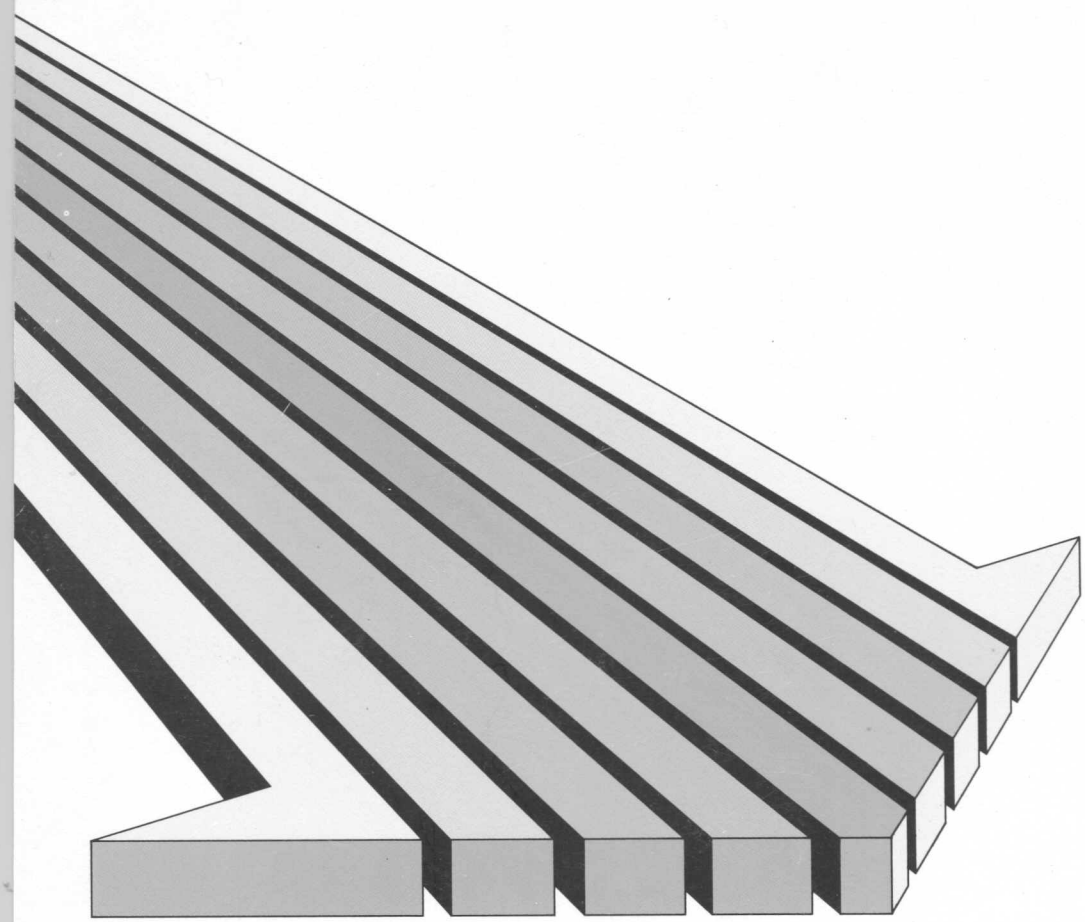
iSBC® 286/10 ES DEVELOPMENT KIT DATA BOOK



iSBC® 286/10 ES DEVELOPMENT KIT
iSBC® 286/10 SINGLE BOARD COMPUTER
iSBC® 028CX, 056CX AND 012CX iLBX™ RAM BOARD
iSDM™ 286 iAPX 286 SYSTEM DEBUG MONITOR

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iSBC® 286/10ES DEVELOPMENT KIT

- **Contains an iSBC® 286/10ES Single Board Computer, an iSBC® 012CXES 512KB RAM board, an iSDM™ 286ES System Debug Monitor, and an iSBC® 286/10ES Kit Documentation Package**
- **Provides a complete execution vehicle for designing iSBC® 286/10 based systems**
- **Provides software downloading and debugging capability via a Series III development system to iSBC® 286ES board link**
- **Demonstrates performance effects of iAPX 286 CPU and iLBX™ architecture extension**

The iSBC® 286/10ES Development Kit is an early availability execution vehicle for iSBC 286/10 board designs. The kit contains an iSBC 286/10ES single board computer, an iSBC 012CXES 512KB RAM board, an iSDM™ 286 system debug monitor, and a documentation package. The iSDM 286ES debug monitor provides the iSBC 286/10ES EPROMs, the interconnect cables and an ISIS diskette containing Series III communication routines. This allows you to develop software on a Series III development system and then download and debug on the iSBC 286/10ES board. Hardware and software evaluation can be performed on this iAPX 286-based computer system. The performance benefits of the iAPX 286 chip and the iLBX™ extended architecture can also be quantified using the iSBC 286/10ES Kit.

iSBC® 286/10ES CPU Board

The iSBC 286/10ES Single Board Computer is a pre-production version of the iSBC 286/10 board. This product is an iAPX 286 based single board computer featuring the iLBX extended MULTIBUS® architecture. The ES board is a multiwire board built with ES components and piggyback emulators in place of unavailable components. These emulators preclude the use of one iSBX™ MULTIMODULE connector. The board functions at a 5 MHz clock rate and does not support the 80287 Numeric Processor. Information on the production iSBC 286/10 board is available in the iSBC 286/10 Single Board Computer data sheet #210838.

iSBC® 012CXES iLBX™ RAM Board

The iSBC 012CXES iLBX RAM board is a pre-production version of the iSBC 012CX iLBX RAM board. The board features 512 Kbytes of high performance dual port error corrected read/write memory. The memory can be accessed by MULTIBUS or the iLBX bus. The iSBC 012CXES board will not meet the iLBX performance specification at 8 MHz. Information on the production iSBC 012CX board is available in the iSBC 028CX/056CX/012CX RAM Board data sheet #210837.

iSDM™ 286ES System Debug Monitor

The iSBC 286ES System Debug Monitor is a pre-production version of the iSDM 286 monitor. This package provides the EPROMs, cables, and ISIS routines necessary to download and debug software from a Series III development system to the iSBC 286/10ES board. The ES monitor is a subset of the full production monitor. Full UDI support and 80287 support will be provided in the production monitor. The ISIS routines are provided on a double-density flexible diskette. Information on the production iSDM 286 monitor is available in the iSDM 286 System Debug Monitor data sheet #210835.

Documentation and iLBX™ Cable

Documentation and an iLBX cable are provided as a separate package in the iSBC 286/10ES Kit. The documentation consists of the iSBC 286/10ES Single Board Computer Design Guide, the iSBC 028CX/056CX/012CX RAM Boards Hardware Reference Manual and the iSDM 286 System Debug Monitor Design Guide.

The iLBX cable provides the connection assembly between the iSBC 286/10ES CPU board and the iSBC 012CXES RAM board.

Other Development Equipment Required

In addition to the iSBC 286/10ES Development Kit, the following equipment may be required for development:

- Series III Development System
- Programming Language Software
- MULTIBUS Cardcage and Power Supply
- CRT Console

Warranty and Repair Services

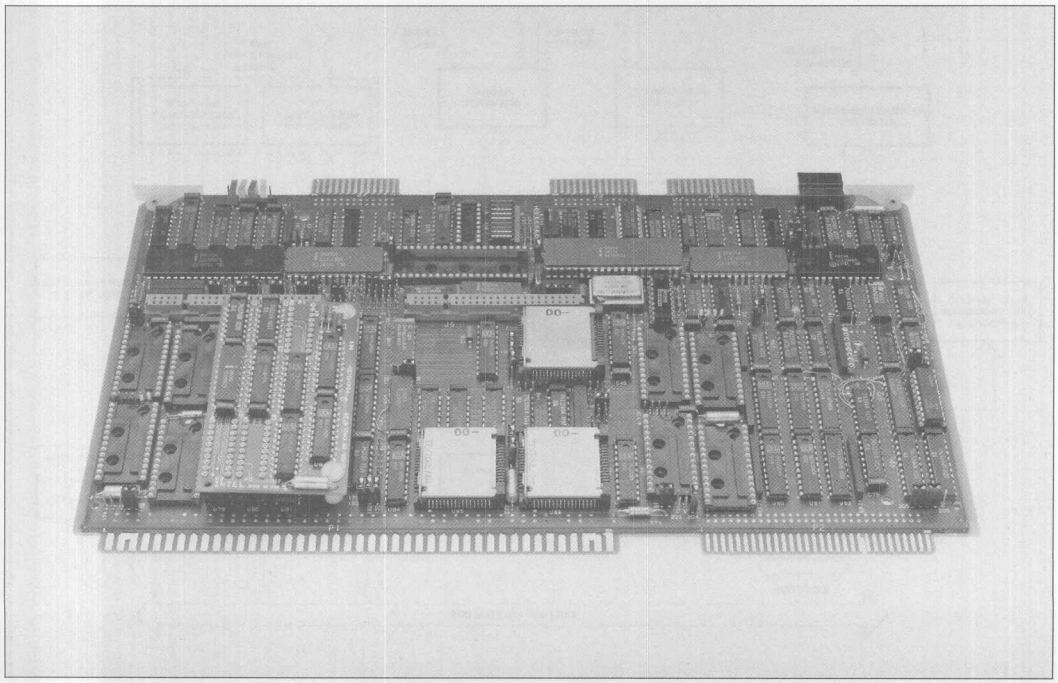
The standard 90 day Intel warranty policy applies to all elements of the iSBC 286/10ES Development Kit allowing full repair, replacement or refund for returned defective product at no charge within 90 days of purchase. Several elements of the kit have specification errata which are documented in the documentation package shipped with the kit. Intel makes no commitments to upgrade this product in the future.

Repair service for the iSBC 286/10ES Development Kit will be provided by the Intel factory, not by the Intel repair center. Information regarding the repair of these products can be attained from your local Intel sales office.

iSBC® 286/10
SINGLE BOARD COMPUTER

- iAPX 286/10 (80286) Microprocessor with 5 or 8 MHz CPU clock
- Optional iAPX 286/20 Numeric Data Processor
- iLBX™ (Local Bus eXtension) interface for high-speed memory expansion
- Two iSBX™ bus interface connectors for I/O expansion
- Eight JEDEC 28-pin sites for optional RAM/iRAM/EPROM/E²PROM components
- Expandable to twelve JEDEC 28-pin sites with addition of an iSBC® 341 28-pin site expansion board
- 16 levels of vectored interrupt control
- A Centronics compatible parallel I/O printer interface
- Two programmable multi-protocol synchronous/asynchronous serial interfaces; one RS232C, the other RS232C or RS422 compatible
- MULTIBUS® interface for multi-master configurations and system expansion

The iSBC® 286/10 Single Board Computer is a member of Intel's complete line of microcomputer modules and systems which take advantage of Intel's technology to provide economical, off-the-shelf, computer-based solutions for OEM applications. The board is a complete computer system on a 6.75 x 12.0 inch printed circuit card. The CPU, system clock, memory sockets, I/O ports and drivers, serial communications interface, priority interrupt logic and programmable timers, all reside on the board.



FUNCTIONAL DESCRIPTION

Overview

The iSBC 286/10 board combines the powerful iAPX 286 CPU with an enhanced MULTIBUS® system architecture, the iLBX™ bus, to provide a high performance 16-bit solution. This board also includes on-board interrupt, memory and I/O features facilitating a complete single board computer system.

Central Processing Unit

The central processor for the iSBC 286/10 board is the iAPX 286 (80286) CPU. The iAPX 286 CPU is upwardly compatible with Intel's iAPX 88 and iAPX 86 CPUs. The iAPX 286 CPU runs iAPX 88 and 86 code at substantially higher speeds due to parallel chip architecture. In addition, the iAPX 286/10 CPU provides on chip memory management and protection and virtual memory addressing of up to one gigabyte per task.

Vectored Interrupt Control

Incoming interrupts are handled by two on-board 8259 programmable interrupt controllers, the interrupt support of the 8274, and by the 80286's NMI line. Interrupts originating from any one of 23 requests are prioritized and then sent to the CPU as a vector address. Jumper stakes allow the user to connect the desired interrupt sources to specific interrupt levels.

Memory Capabilities

There are eight 28-pin JEDEC sites on board which may contain a combination of byte-wide devices including RAM, iRAM, EPROM, and E^2PROM. These sites are organized into two 4-site blocks, one of which may be dual-ported. The dual port block may be extended to eight sites (i.e. 12 sites total) by the addition of an iSBC 341 JEDEC site expansion module. The on-board EPROM capacity using twelve 27128 EPROMs is 192 Kbytes. The on-board RAM using ten 2186 iRAMs is 80 Kbytes.

I/O Capabilities

On-board I/O is based on three Intel IC's: the 8255 parallel I/O controller, the 8274 serial I/O chip and the 8254 event timers chip. The parallel I/O interface is used to control some on-board functions as well as provide for

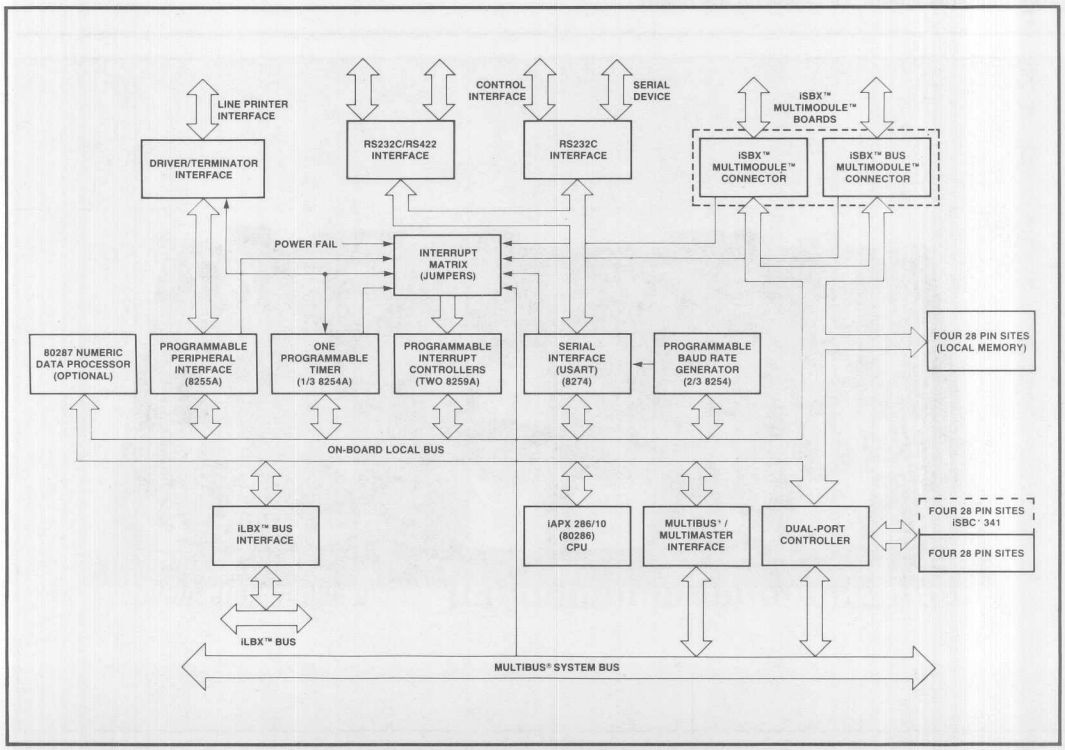


Figure 1. iSBC® 286/10 Block Diagram

a Centronics compatible printer port. Two serial channels are supported. One channel may be either RS232 or RS422 with the other channel RS232 only. Three interval timers are available, one of which is used for programmable baud rate generation for the serial channels.

iSBX™ Interface

The iSBX™ bus interface is an I/O expansion bus intended to increase the functionality of a CPU board at a minimal cost. Two 16-bit iSBX MULTIMODULE™ connectors are provided on the iSBC 286/10 board. One of these connectors can accept a single width MULTIMODULE and the other can accept either a single-wide or a double-wide MULTIMODULE.

Enhanced iLBX™ BUS System Architecture

The iSBC 286/10 board also provides the local bus extension (iLBX) of the MULTIBUS interface. This standard extension allows on-board memory performance with physically off-board memory. The iLBX is implemented over the P2 connector and requires cabling across the "virtual" SBCs of a system (see Figure 2). Other Intel products which support the iLBX bus include:

iSBC 028CX 128Kb iLBX RAM board

iSBC 056CX 256Kb iLBX RAM board

iSBC 012CX 512Kb iLBX RAM board

iSBC 428 JEDEC 28-PIN SITE board

iSBC 580 MULTICHANNEL™ INTERFACE board

Full MULTIBUS multimaster control is supported by the iSBC 286/10 board. Other MULTIBUS compatible CPU, memory and I/O boards may be added to a system to extend its functionality.

Software Support

Real-time multi-user support for the iSBC 286/10 board is provided by the iRMX™ 286R Operating System (available Q2, 83). iRMX 286R provides a modified iRMX 86 nucleus to operate on the iSBC 286/10 board in real address mode, enhances the ICU for configuration support of the board, adds a driver for the on-board 8274 and supports the 80287. iRMX 86 Release 5 is a prerequisite for iRMX 286R.

Interactive multi-user support is provided by the XENIX[1] operating system (available Q3, 83). XENIX is a compatible derivative of UNIX[2], System III.

Language support for the iSBC 286/10 board's real address mode includes Intel's ASM 86, PL/M 86, PASCAL and FORTRAN as well as many third party 8086 languages. Language support for virtual address mode operation includes ASM 286 and PL/M 286 with PASCAL and C available in the second half of 1983. Programs developed in these languages can be downloaded from an Intel Series III Development System to the iSBC 286/10 board via the iSDM 286 System Debug Monitor (available Q3, 83).

[1] XENIX is a trademark of Microsoft Inc.
[2] UNIX is a trademark of Bell Labs.

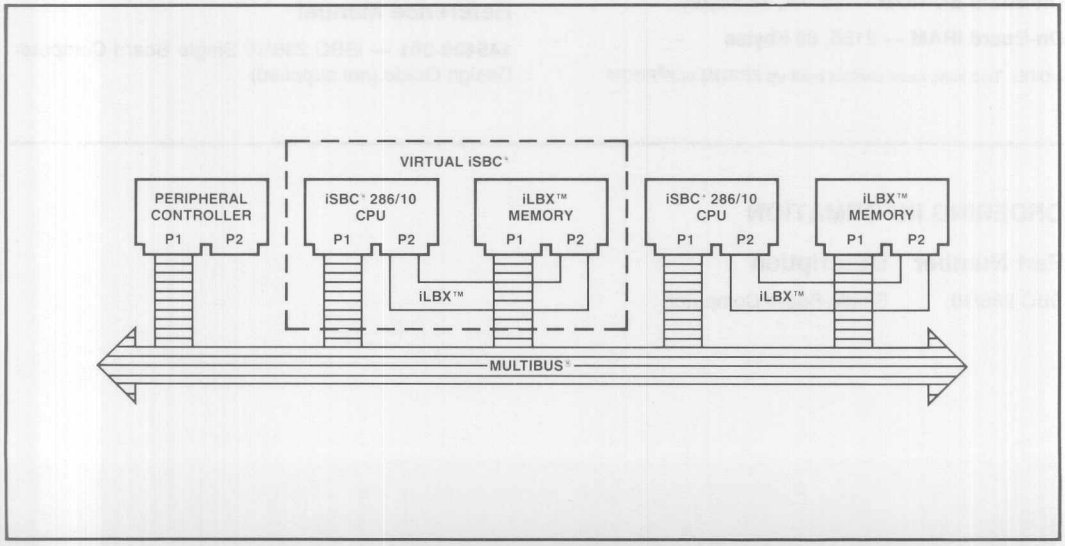


Figure 2. MULTIBUS®/iLBX™ Configuration

SPECIFICATIONS

Word Size

Instruction — 8, 16, 24, 32 or 40 bits

Data — 8 or 16 bits

System Clock

5.0 or 8.0 MHz

Cycle Time

Basic Instruction — 8 MHz — 375 ns, 250 ns (assumes instruction is in queue); 5 MHz — 600 ns, 400 ns (assumes instruction is in queue)

NOTE: Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles)

Memory Capacity (Memory ICs Not Included)

On-Board EPROM — 2716, 16Kbytes; 2732, 32 Kbytes; 2764, 64 Kbytes; 27128, 128 Kbytes

On-board E^2PROM — 2817A, 16 Kbytes

On-Board iRAM — 2186, 48 Kbytes

NOTE: Two sites must contain boot-up EPROM or E^2PROM

With One iSBC® 341 MULTIMODULES™

On-Board EPROM — 2716, 24 Kbytes; 2732, 48 Kbytes; 2764, 96 Kbytes; 27128, 192 Kbytes;

NOTE: Dual port sites can address 128 Kbytes of memory maximum

On-Board E^2PROM — 2817A, 24 Kbytes

On-Board iRAM — 2186, 80 Kbytes

NOTE: Two sites must contain boot-up EPROM or E^2PROM

I/O Capability

Parallel — 12 programmable lines using one 8255A

Serial — 2 programmable lines using one 8274

Timers — 3 programmable timers using one 8254

Expansion — 2 iSBX MULTIMODULE connectors

Interrupt Capability

Interrupt Sources — 30 sources, jumper selectable

Interrupt Requests — 23 vectored requests using two 8259s, an 8274, and the 80286's NMI line

Physical Characteristics

Width — 12.00 in. (30.48 cm)

Height — 6.75 in. (17.15 cm)

Depth — 0.70 in (1.78 cm)

Weight — 14 oz. (388 gm)

Electrical Characteristics/DC Power Requirements

+5V, 6.5A; +12V, 50 mA; −12V, 50 mA

NOTE: Does not include power for optional EPROM, E^2PROM, or RAM

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Relative Humidity — to 90% (without condensation)

Reference Manual

145439-001 — iSBC 286/10 Single Board Computer Design Guide (not supplied)

ORDERING INFORMATION

Part Number	Description
SBC 286/10	Single Board Computer

iSBC® 028CX, 056CX, AND 012CX iLBX™ RAM BOARDS

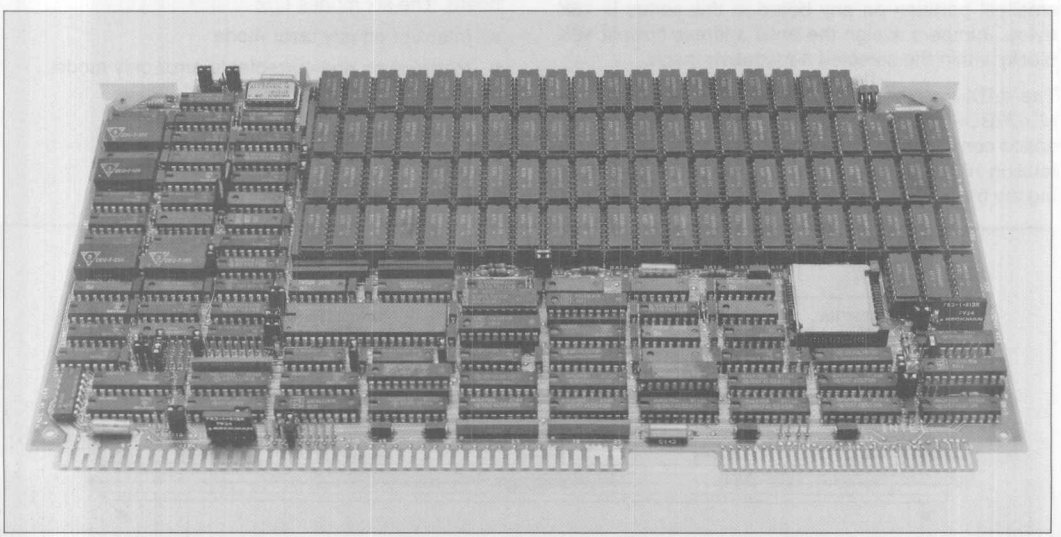
- **Dual port capability via MULTIBUS® and iLBX™ Bus Interfaces**
- **Single bit error correction and double bit error detection via Intel 8206 ECC device**
- **128K byte, 256K byte and 512K byte versions available**
- **Control status register supports multiple ECC operating modes**
- **Error status register provides error logging by host CPU board**
- **16 megabyte addressing capability with base address selectable on 16K byte boundaries**
- **Supports 8- or 16-bit data transfer and 24-bit addressing**
- **Auxiliary power bus and memory protect logic for battery back-up RAM requirements**

The iSBC® 028CX, iSBC 056CX, and iSBC 012CX RAM memory boards are members of Intel's complete line of iSBC memory and I/O expansion boards. Each board interfaces directly to any iSBC 80, iSBC 88, iSBC 86, iSBC 186 and iSBC 286 Single Board Computers. The dual port feature of the CX series of RAM-boards allows access to the memory of both the MULTIBUS® and the iLBX™ interfaces.

In addition to the dual port features the "CX" series of RAM-boards provide Error Correction Circuitry (ECC) which can detect and correct single bit errors and detect, but not correct, double and most multiple bit errors.

The iSBC 028CX, iSBC 056CX and iSBC 012CX boards contain 128K, 256K or 512K bytes of read/write memory using 64K dynamic RAM components.

Due to the iLBX dual port capability and on-board ECC features of the board they are ideally suited in applications where memory performance and integrity of the stored data is critical, such as financial transactions, process control and medical equipment applications.



FUNCTIONAL DESCRIPTION

General

The iSBC 028CX, 056CX and 012CX RAM boards are physically and electrically compatible with the MULTIBUS interface standard, IEEE P796, as outlined in the Intel MULTIBUS specification. In addition the CX series of RAM-boards are physically and electrically compatible with the iLBX bus interface as outlined in the Intel iLBX Specification.

Dual Port Capabilities

The "CX" series of RAM-boards can be accessed by either the MULTIBUS interface or the iLBX interface. Intel's new Local Bus Extension interface (iLBX bus) is an unarbitrated bus architecture which allows direct transfer of data transfer between the CPU and the memory boards without accessing the MULTIBUS. Due to the unarbitrated nature of the iLBX interface significant improvements in memory access times result, typically 350% to 400%, over MULTIBUS memory access times.

System Memory Size

Maximum system memory size with this series of boards is 16 megabytes. Memory partitioning is independant for the MULTIBUS interface and the iLBX interface.

For MULTIBUS operations, on-board jumpers assign the board to one of four 4-megabyte pages. Each page is partitioned into 256 blocks of 16K bytes each. The smallest partition on any board in this series is 16K bytes. Jumpers assign the base address (lowest 16K block) within the selected 4-megabyte page.

The iLBX bus memory partitioning differs from the MULTIBUS partitioning in that the iLBX bus address space consists of 256 contiguous blocks of 64K bytes totaling 16 megabytes. As with the MULTIBUS partitioning the base addresses are set with on-board jumpers.

Error Checking and Correcting (ECC)

Error checking and correction is accomplished with the Intel 8206 Error Checking and Correcting device. This ECC component in conjunction with the ECC check bit RAM array provides error detection and correction of single bit errors and detection only of double bit and most multiple bit errors. The ECC circuitry can be programmed via the Control Status Register (CSR) to various modes while error logging is supported by the Error Status Register (ESR). Both CSR and ESR communicate with the master CPU board through a single I/O port.

ECC I/O ADDRESS SELECTION

The processor board communicates with the ECC circuitry via a single I/O port. This port is used for the Control Status Register (CSR) and the Error Status Register (ESR). The CSR is programmed by the user to determine the mode of operation while the ESR provides information about memory errors. The iSBC 028CX, iSBC 256CX and iSBC 012CX RAM boards are shipped with a Programmed Array Logic (PAL) device which allows selecting one of 9 possible addresses for the I/O port. The actual selection is done by jumper configuration. Additional unprogrammed locations are left in the PAL to allow application specific I/O addresses to be defined.

CONTROL STATUS REGISTER

There are six ECC modes of operation in the "C" Series family of RAM boards. Each mode is obtained by software programming of the CSR from the master iSBC board. The six modes are:

a. Interrupt on any error mode
b. Interrupt on non-correctable error only mode
c. Correcting mode
d. Non-correcting mode
e. Diagnostic mode
f. Examine syndrome word mode

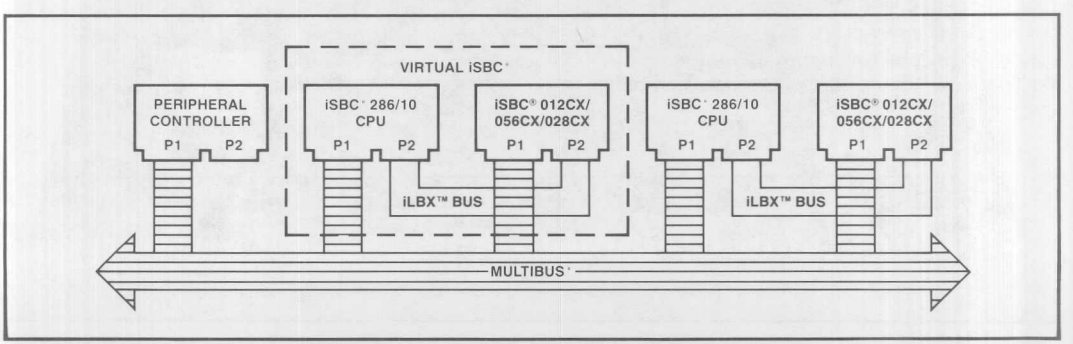


Figure 1. Typical iLBX™ System Configuration

Modes (a) and (b) can be used in conjunction with (c) and (d). The six modes are described below.

Interrupt on Any Error Mode — In this mode the RAM board will interrupt the iSBC processor board when any error (single bit or multiple bit) is detected by the ECC circuitry.

Interrupt on Non-Correctable Error Mode — In this mode the RAM board will interrupt the iSBC processor board only when a non-correctable (multiple bit) error is detected by the ECC circuitry. A multiple bit error is not correctable by the ECC circuitry.

Correcting Mode — In this mode the RAM board corrects any correctable error (single bit error). Errors which are not correctable are not modified. Interrupts are generated depending on the interrupt mode selected.

Non-Correcting Mode — In this mode the RAM board does not correct any error. The ECC circuitry continues to check for errors, but no corrective action is taken. Interrupts continue as described previously.

Diagnostic Mode — This mode is used for testing the on-board ECC circuitry. In this mode the write enable strobe to the ECC RAM array is continuously disabled. The diagnostic mode can be used to simulate errors and in conjunction with the "Examine Syndrome Word Mode" examine the check bits generated by the ECC circuitry.

Examine Syndrome Word Mode — This mode, in conjunction with the diagnostic mode, is used for testing the ECC memory. In this mode, the syndrome bits/check bits are clocked into the ESR on every memory read/write cycle, respectively. The ESR translation PROM switches to a transparent mode in the examine syndrome word mode. This allows the actual syndrome word generated by the 8206 ECC device to be examined.

ERROR STATUS REGISTER

This 8-bit register contains information about memory errors. The ESR reflects the latest error occurence. Table 1 shows the status register format. Bits 5 and 6 show the failing row while bits 0 through 4 indicate which bit (of the 16-bit data word or the 6-bit ECC syndrome word) is in error. Bit 7 is always high.

Bit 6	Bit 5	Meaning	
0	0	Error in row	0
0	1		1
1	0		2
1	1		3

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Meaning	
0	0	0	0	0	Error in data bit	0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0		8
0	1	0	0	1		9
0	1	0	1	0		10
0	1	0	1	1		11
0	1	1	0	0		12
0	1	1	0	1		13
0	1	1	1	0		14
0	1	1	1	1		15
1	0	0	0	0	Error in check bit	0
1	0	0	0	1		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
1	0	1	0	1		5
1	1	1	1	0	No Error	
1	1	1	1	1	Non-correctable (multiple-bit error)	

NOTE: Bit 7 is always high

Table 1. Error Status Register Format

Battery Back-up/Memory Protect

An auxillary power bus is provided to allow separate power to the RAM array for systems requiring backup of read/write memory. An active low TTL compatible memory protect signal is brought out on the auxillary bus connector which, when asserted, disables read/write access to the RAM board. This input is provided for the protection of RAM contents during system power-down sequences.

SPECIFICATIONS

Word Size Supported

8- or 16-bits

Memory Size

131,072 bytes (iSBC 028CX board)

262,144 bytes (iSBC 056CX board)

524,288 bytes (iSBC 012CX board)

Access Times (All densities)

MULTIBUS®

Read/Full Write — 350 ns (max)

Write Byte — 530 ns (max)

iLBX™ BUS

Read/Full Write — 300 ns (max)

Write Byte — 440 ns (max)

Cycle Times (All densities)

MULTIBUS®

Read/Full Write — 460 ns (max)

Write Byte — 885 ns (max)

iLBX™ BUS

Read/Full Write — 375 ns

Write Byte — 740 ns

NOTE: If an error is detected, read access time and cycle times are extended to 255 ns (max)

Refresh Cycle Time — 15.6 μs

Refresh Delay Time — 760 ns

Memory Partitioning

Maximum System memory size is 16M Bytes for both MULTIBUS and iLBX BUS. MULTIBUS partitioning is by Page, Block and Base, while the iLBX BUS is by Block and Base only.

PAGE ADDRESS

MULTIBUS® — 0-4 megabytes; 4-8 megabytes; 8-12 megabytes; 12-16 megabytes

iLBX™ BUS — N/A

BLOCK ADDRESS

Board	MULTIBUS® (16K Bytes)	iLBX™ Bus (64K Bytes)
iSBC® 028C	8 contiguous 16K byte blocks	2 blocks of 64K bytes
iSBC® 056C	16 contiguous byte blocks	4 blocks of 64 bytes
iSBC® 012C	32 contiguous 16K byte blocks	8 blocks of 64K bytes

NOTE: Blocks cannot cross 4M byte boundary

BASE ADDRESS

MULTIBUS® — Any 16K byte boundary

iLBX™ BUS — Any 64K byte boundary

Power Requirements

Voltage — 5VDC $\pm$ 5%

Board	Current	Standby (Battery Backup)
iSBC® 028CX	3.8A (typ.) 6.5A (max.)	2.0A (typ.) 2.2A (max.)
iSBC® 056CX	4.0A (typ.) 6.6A (max.)	2.1A (typ.) 2.3A (max.)
iSBC® 012CX	4.4A (typ.) 6.8A (max.)	2.3A (typ.) 2.5A (max.)

Environmental Requirements

Operating Temperature — 0°C to 55°C

Operating Humidity — To 90% without condensation

Physical Dimensions

Width — 30.48 cm (12 inches)

Height — 17.15 cm (6.75 inches)

Thickness — 1.27 cm (0.50 inches)

Weight — iSBC 028CX: 4699 gm (16.7 ounces); iSBC 056CX: 5329 gm (19.0 ounces); iSBC 012CX: 6589 gm (23.5 ounces)

Reference Manuals

145158-001 — iSBC 028CX/iSBC 056CX/iSBC 012CX Hardware Reference Manual

144456-001 — Intel iLBX Specification

9800683-03 — Intel MULTIBUS Specification

Manuals may be ordered from any Intel Sales Representative, Distributor Office or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

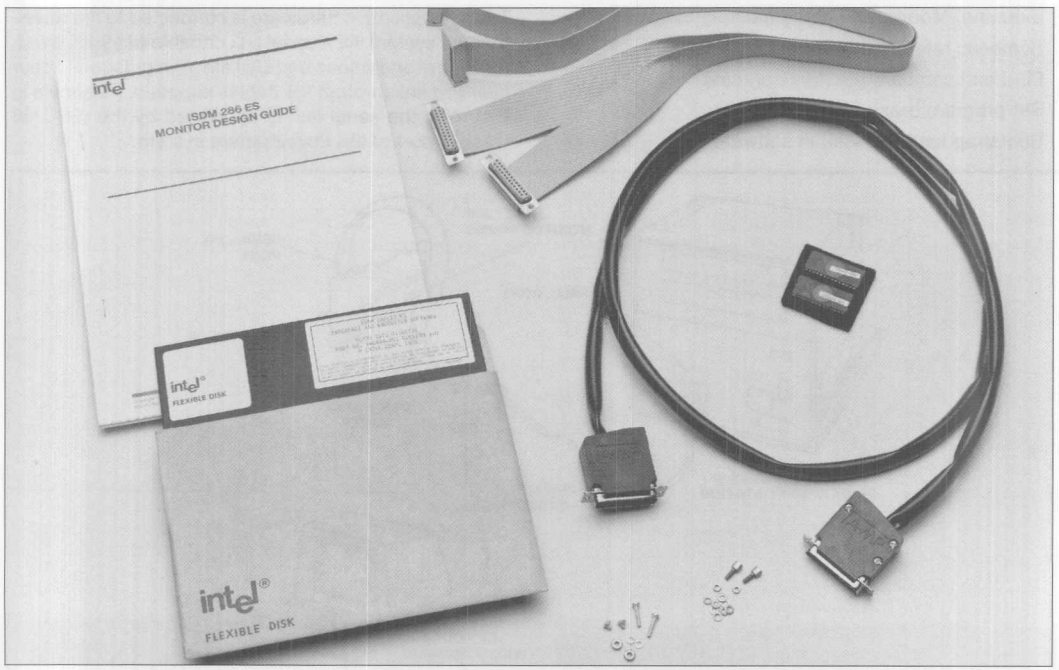
ORDERING INFORMATION

Part Number	Description
iSBC 012CX	512K byte RAM board with iLBX
iSBC 056CX	256K byte RAM board with iLBX
iSBC 028CX	128K byte RAM board with iLBX

iSDM™ 286
iAPX 286 SYSTEM DEBUG MONITOR

- **Development support of iAPX 286- and iSBC® 286-based applications**
- **Real Address Mode (ram) and Protected Virtural Address Mode (pvam) support**
- **Universal Development Interface (UDI) support via development system connection**
- **Underlying debugging tool for iRMX™ 286R applications**
- **Supports 80287 Numeric Processor Extension (NPX) for high-speed math applications**
- **Program load capability from Intellec® Series III Development Systems**
- **Bootstrap Loader for iRMX™ 86, 88, and 286R file compatible peripherals**
- **iAPX 286 single step operation allowed**

The Intel iSDM 286 System Debug Monitor package contains the necessary hardware, software, cables, PROMs, and documentation required to interface an iAPX 286 component or iSBC 286 board applications to an Intellec Series III through a high-speed link. The System Debug Monitor supports an OEM's choice of custom operating system, or the iRMX 286R Real-Time Multi-Tasking Operating System with debugging tools to examine CPU registers, memory content, CPU descriptor tables, and other crucial environmental details. The Monitor also allows programs to access files on the development system via the internal UDI support and the serial communication link.



FUNCTIONAL DESCRIPTION

Overview

The iSDM 286 System Debug Monitor provides programmers of iAPX 286-based applications with the debugging tools needed to test new applications ranging from single-user systems to complex operating systems. Programmers are given direct access to both the Real Address (ram) and Protected Virtual Address (pvam) Modes of the CPU via a simple terminal interface, or via an Intellec Series III Development System.

Universal Development Interface

Any iRMX 86, Series III, or other UDI-based application can be supported by the iSDM 286 Monitor. The Monitor emulates many of the UDI calls (ram or pvam), and passes all requests for a file system to the host development station. UDI applications such as compilers and other programs available from Independent Software Vendors can be tested in the target iAPX 286 environment immediately.

Powerful Debugging Commands

A powerful set of user functions includes commands to:

Examine and Modify CPU Registers
Examine, Modify, and Move memory locations
Symbolic reference to variable names
Find and compare memory contents
Set program breakpoints
Bootstrap load application software
Single-step CPU operation
Change between Real Address Mode and Protected Virtual Address Mode

Formatted Displays

The iSDM 286 Monitor formats all iAPX 286 pre-defined data structures into clearly understandable displays. This display gives programmers a formatted view of CPU registers such as LDTs, GDTs, IDTs, Segment Selectors, and Task State Segments — not just a series of unconnected digits.

Numeric Data Processor Support

In addition to executing 80287 Numeric Processor Extension (NPX) applications with full NPX performance, programmers may examine and modify NPX registers using decimal and real number format. Any location in memory known to contain numeric values in standard real format (IEEE P754) may be examined or modified using normal decimal notation. In this manner programmers may feel confident that correct and meaningful numbers are available to applications without having to encode and decode complex real, integer, and BCD hexadecimal formats.

High-Speed Serial Connection

Target application hardware is connected to the development system via a serial link capable of 19.2K baud. All control operations and UDI file manipulations occur over this link through the cables supplied. As shown in Figure 1, the serial link is supported by the iSBC 86 USART port of the development system.

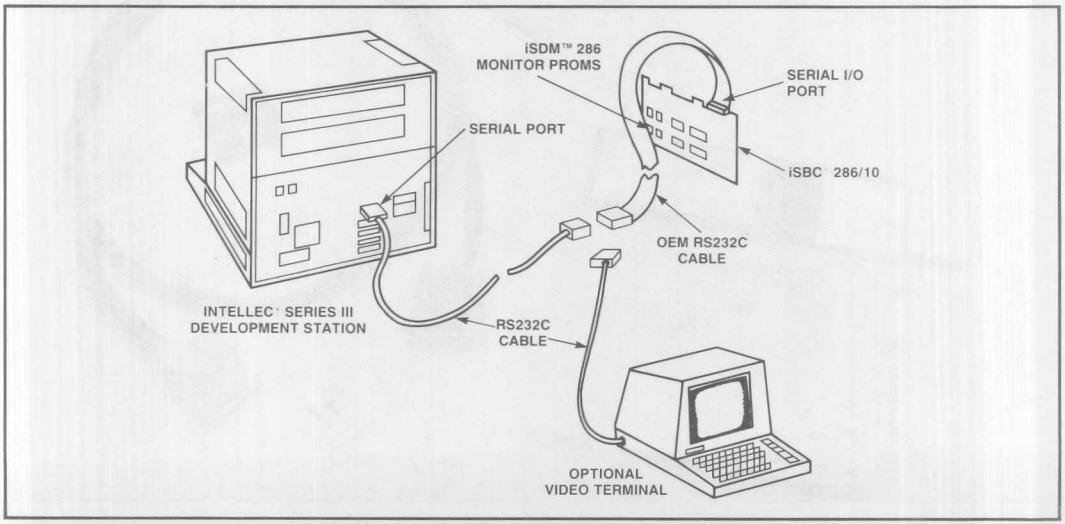


Figure 1. Typical iSDM™ 286 Environment

AFN-01804A

SPECIFICATIONS

Development System Environment

Intellec MDS Series III with 64 KBytes.

Target System Environment

Any iAPX 286 system with 8274 (non-vectored mode) serial link, 8254 timer, and 8259A interrupt controller such as the iSBC 286/10 Single Board Computer.

PROMs are supplied for locations 0FF8000H through 0FFFFFFH.

ORDERING INFORMATION

Part Number	Description
SDM 286	iAPX 286 and iSBC 286 System Debug Monitor package including cables, PROMs, software, and operator manual A software license must be or have been executed